Claims

[c1] 1. A method of forming a precision element on a semiconductor substrate comprising the steps of:
forming a first element in a first region of a semiconductor substrate;
forming a plurality of second elements in a second region of the substrate, the plurality of second elements comprising individual elements, the individual elements ranging in value about a desired value;
measuring the value of the first element;
comparing the measured value to a target value; and
selecting at least one the individual second elements corresponding to the result of the comparison.

[c2] 2. The method of Claim 1 wherein the plurality of second elements comprise one element having a nominal value about equal to the desired value, another element having a value of about 10 % less than the desired value, and a further element having a nominal value of about 10 % greater than the value of the desired element.

[c3] 3. The method of Claim 2 wherein when the measured value of the first element is greater than the target value, the element having a nominal value of about 10 % less

than the desired value is selected.

[c4] 4. The method of Claim 2 wherein when the measured value of the first element is less than a predetermined target value, the element having a nominal value of about 10 % greater than the desired value is selected.

[c5] 5. The method of Claim 2 wherein when the measured value of the first element is equal to the predetermined target value, the element having a value about equal to the value is selected.

[c6] 6. The method of Claim 1 wherein the first and the second elements include a passive element selected from the group consisting of a resistor, a capacitor, a diode and a transistor.

[c7] 7. The method of Claim 1 wherein the first and the second elements are resistors.

[c8] 8. The method of Claim 1 wherein said plurality of second elements is arranged in parallel to each other.

[c9] 9. The method of Claim 1 wherein said plurality of second elements comprise three resistors that are arranged in parallel to each other.

[c10] 10. The method of Claim 1 wherein said plurality of second element is linked by fusible links or antifuses.

[c11] 11. The method of Claim 1 wherein said comparing is performed manually or electronically.

[c12] 12. The method of Claim 1 wherein the selecting includes a step of removing other second elements that are not selected by blowing fusible links or by fusing antifuses that are present within said plurality of second elements.

[c13] 13. A precision passive circuit structure comprising:
a first passive element located in a first region of a semiconductor substrate; and
a plurality of second passive elements located in a second region of the semiconductor substrate, wherein the second passive elements are arranged in a parallel configuration and each second passive element has a nominal value that ranges about a desired value.

[c14] 14. The precision passive circuit structure of Claim 13 wherein the plurality of second passive elements comprise one element having a nominal value about equal to the desired value, another element having a nominal value of about 10 % less than the desired value, and a further element having a nominal value of about 10 % greater than the desired value.

[c15] 15. The precision passive circuit structure of Claim 13

wherein the first and the second passive elements are selected from the group consisting of a resistor, a capacitor, a diode and a transistor.

[c16] 16. The precision passive circuit structure of Claim 13 wherein the first and the second passive elements are resistors.

[c17] 17. The precision passive circuit structure of Claim 13 wherein said plurality of second elements comprise three resistors.

[c18] 18. The precision passive circuit structure of Claim 15 wherein said plurality of second passive elements are linked by fusible links or antifuses.